Chunghwa Picture Tubes, Ltd.
Technical Specification

To : **General**
Date : **2012/02/06**

CPT TFT-LCD
CLAA133UA03

APPROVED BY	CHECKED BY	PREPARED BY
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Modification Record List

NO.	Issue Date	Modification Index
1	2012/02/06	Tentative version
2		
3		
4		
5		
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7		
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10		

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1. OVERVIEW

CLAA133UA03 is 13.3" color (16：9) TFT-LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel, LVDS driver ICs, control circuit and backlight. By applying 6 bit digital data, 1600×RGB (3) ×900, 262K-color images are displayed on the 13.3" diagonal screen. General specifications are summarized in the following table：

ITEM	SPECIFICATION
Display Area	293.28(H) x 164.97(V) (㎜) (13.3-inch diagonal)
Number of Pixels	1600 x 3 (RGB) x 900
Pixel Pitch	0.1833 (H) x 0.1833 (V) (mm)
Color Pixel Arrangement	RGB vertical stripe
Display Mode	Normally white
Number of Colors	262,144(6bits) (LVDS)
Gamut	42%(min)/45% (Typ)
Optimum Viewing Angle	6 o'clock
Response Time	16ms (Typ)
Surface Treatment	AG25%
Viewing Angle	80°、-80° /60°、-80° (min.)
Brightness	290 cd/m^2 (5point) (Typ) 250 cd/m^2 (5point) (Min)
Uniformity	5point：80% 13point：65%
Consumption of Power	3.9W (Max)
Module Size	306.3(W)x 195.27(H)x3.0(D) (mm) (Max)
Module Weight	(240)g (Max)

The LCD Products listed on this document are not suitable for use of aerospace equipment, submarine cable, and nuclear reactor control system and life support systems. If customers intend to use these LCD products for applications listed above or those not included in the "Standard" list as follows, please contact our sales in advance.

Standard：Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tool, Industrial robot, Audio and Visual equipment, Other consumer products.

2. ABSOLUTE MAXIMUM RATINGS

The following are maximum value, which if exceeded, may cause faulty operation or damage to the unit.

ITEM	SYMBOL	MIN	MAX	UNIT	NOTE
LCD Power Voltage	VCC	0	4.0	V	
LED Driver Input Voltage	VBL+	7	21	V	
Operation Temperature	Top	0	50	℃	*1).*2).*3).*4).
Storage Temperature	Tstg	-25	65	℃	*1).*2).*3).

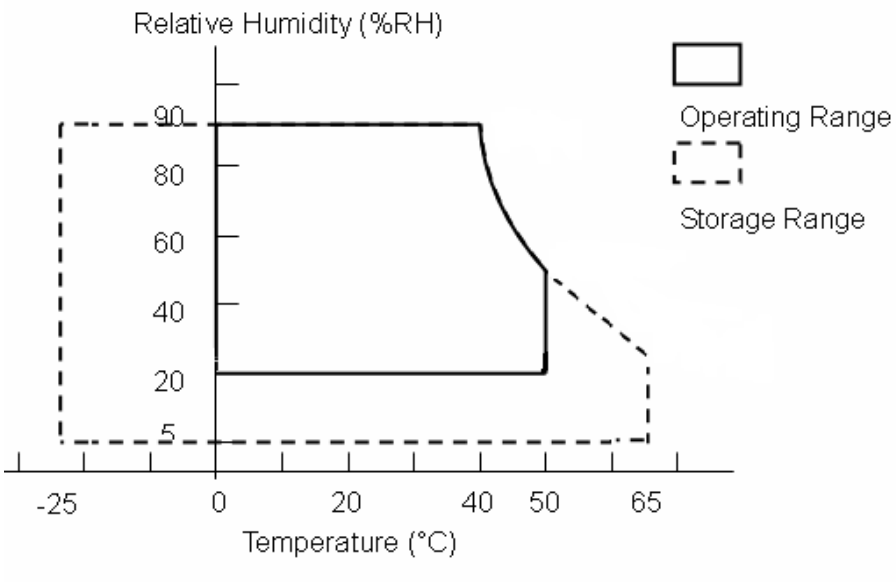
【Note】

*1) The relative temperature and humidity range are as below sketch, 90%RH Max. (Ta≦40℃)

*2) The maximum wet bulb temperature ≦39℃(Ta＞40℃) and without dewing.

*3) If product in environment which over the definition of the relative temperature and humidity out of range too long, it will affect visual of LCD.

*4) If you operate LCD in normal temperature range, the center surface of panel should be under 50℃.



3. ELECTRICAL CHARACTERISTICS

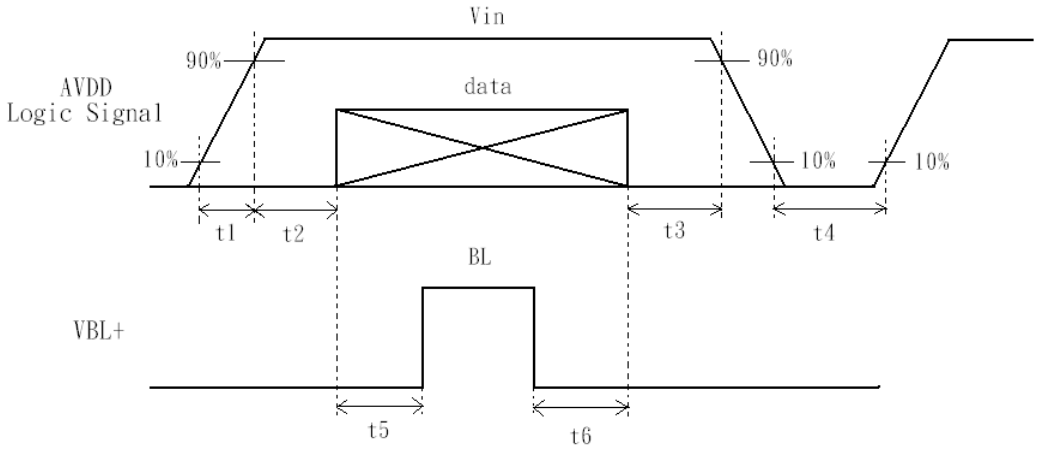
(A) TFT LCD

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
LCD Power Voltage	VCC	3.0	3.3	3.6	V	*1)
LCD Power Current	ICC	-	320	400	mA	*2)
Rush Current	Irush	-	-	2	A	*4)

【Note】

*1)

(a) Power Sequence：



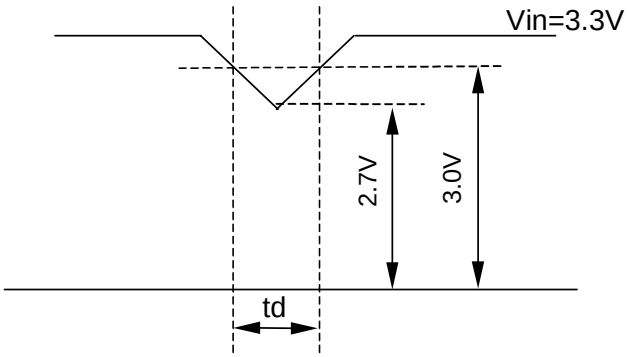
data:RGB DATA, DCLK, HD, VD, DENA

0.50 ms≦t1 ≦10 ms
0.01 ms＜t2 ≦50 ms
0.01 ms＜t3 ≦50 ms
500 ms≦t4
200 ms≦t5
200 ms≦t6

(b)VCC-dip state

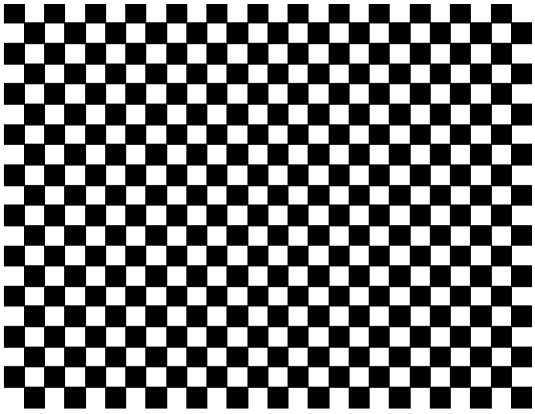
(1)when 3.0V＞VCC≧2.7V，td≦10 ms.

(2)when VCC＜2.7V，VCC-dip condition should as the VCC-turn-off condition.



*2) Typical value is Mosaic (32*36 Checker board) Pattern：900 line mode.

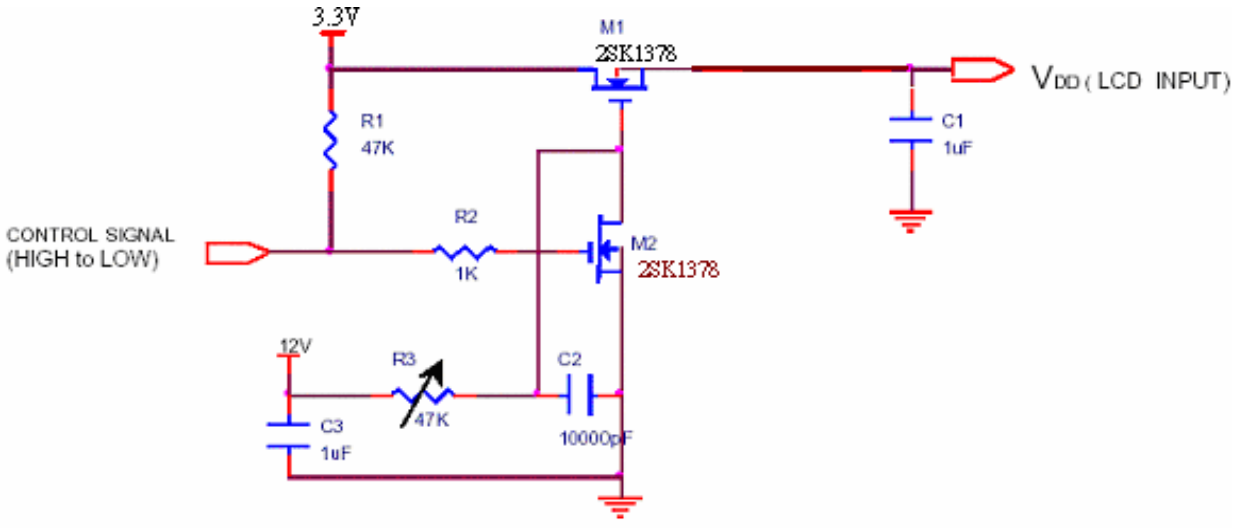
Circuit condition (Typ)：VCC=3.3 V，f_V=60 Hz，f_H = 55.56 KHz，f_{CLK} = 97.78MHz

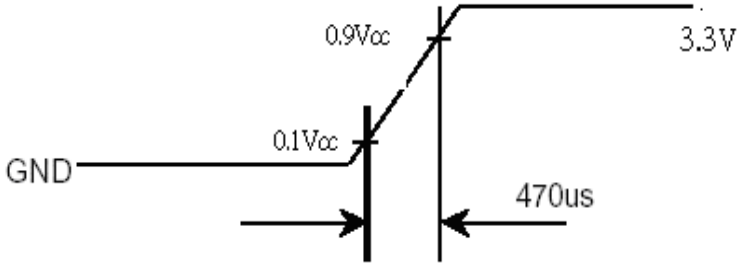


Max value is Black Pattern：900 line mode.

Circuit condition (Max)：VCC=3.3 V，f_V=60 Hz ，f_H = 55.56 KHz，f_{CLK} = 97.78 MHz

*3) Irush measure condition


3.3V
M1
2SK1378
VDD (LCD INPUT)
R1
47K
C1
1uF
CONTROL SIGNAL
(HIGH to LOW)
R2
1K
M2
2SK1378
12V
R3
47K
C2
10000pF
C3
1uF


0.9Vcc
3.3V
0.1Vcc
GND
470us

(B) BACK LIGHT

(a.) ELECTRICAL CHARACTERISTICS

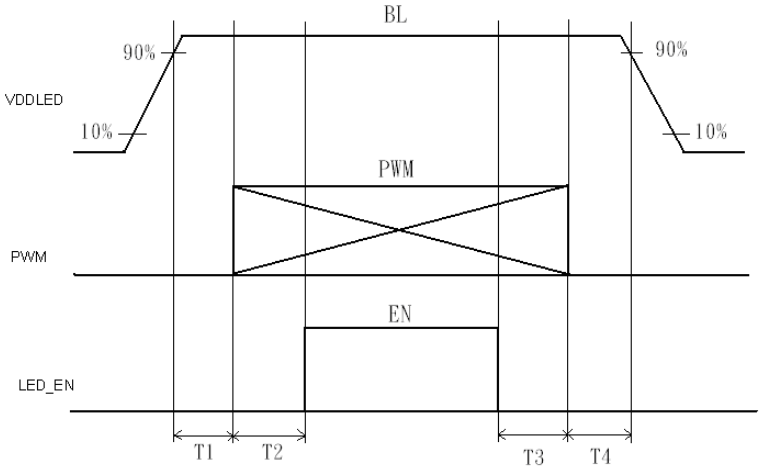
Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
LED Driver Input Voltage	VBL+	7	12	21	V	
LED Driver Input Current	IBL+			(450)	mA	*1)
Forward Voltage	VF		2.9	3.0	V	*2) IF=20mA
Forward Current	I_F	18	20	22	mA	*2)
Power Consumption	PLED	2.66	2.73	2.9	W	*2)*3)
PWM Frequency	PWM_BL	180	200	(1K)	Hz	*2)I_F=20mA
Duty ratio	Dim	5		100	%	

(b.) LED LIFE – TIME

ITEM	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Life Time	IF=20mA、Ta=25℃	15000			hrs	*4)

(c.) LED ON/OFF Sequence



0.5ms ≦ T1 ≦10ms

10ms ≦ T2

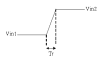
10ms ≦ T3

0ms ≦ T4

10ms ≦ T5

(d.). When LED input voltage is from Vin1 up to Vin2, the slew rate should be less than 20 V/ms.

Slew rate = (Vin2-Vin1) / Tr, Vin2 > Vin1

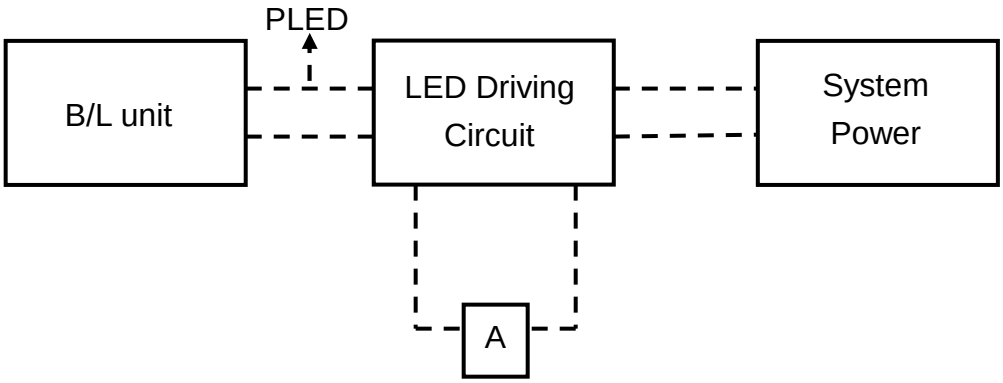


【Note】

*1) Maximum LED Driver Input Current at 7V Input Voltage/PWM Duty 100%.

*2) Measure method：a. LED current is measured by utilizing a current meter as show below.

b. System power PLED is measured at input voltage 12V.



*3) Calculator value for reference $I_F \times V_F \times N = PLED$

*4) Life time means that estimated time to 50% degradation of initial luminous intensity.

4. Connector Interface PIN & Function

(1) CN (Input interface signal)

Input Connector	型式	20455-030E-12(I-PEX) or equivalent 30 pin connector	
Pin assignment	Pin	Signal	Description
	1	NC	Reserved
	2	H_GND	High Speed Ground
	3	LAN1_N	Complement Signal Link Lane 1 (NC_ Reserved for test)
	4	LAN1_P	True Signal Link Lane 1 (NC_Reserved for test)
	5	H_GND	High Speed Ground
	6	LAN0_N	Complement Signal Link Lane 0
	7	LAN0_P	True Signal Link Lane 0
	8	H_GND	High Speed Ground
	9	AUX_P	True Signal Auxiliary Ch.
	10	AUX_N	Complement Signal Auxiliary Ch.
	11	H_GND	High Speed Ground
	12	LCD_VCC	LCD logic and driver power (Power Supply, 3.3 V typical)
	13	LCD_VCC	LCD logic and driver power (Power Supply, 3.3 V typical)
	14	NC	Reserved (BIST function)
	15	LCD_GND	LCD logic and driver ground
	16	LCD_GND	LCD logic and driver ground
	17	NC or HPD	HPD signal pin (Optional in sink device) (2.4V~2.6V)
	18	BL_GND	Backlight ground
	19	BL_GND	Backlight ground
	20	BL_GND	Backlight ground
	21	BL_GND	Backlight ground
	22	BL_ENABLE	Backlight On/Off enable pin (+3.3V Input)
	23	BL_PWM_DIM	System PWM signal input for dimming (+3.3V Swing)
	24	NC	Reserved (For EDID SCL)
	25	NC	Reserved (For EDID SDA)
	26	BL_PWR	Backlight power (5.8V – 21V LED power)
	27	BL_PWR	Backlight power (5.8V – 21V LED power)
	28	BL_PWR	Backlight power (5.8V – 21V LED power)
	29	BL_PWR	Backlight power (5.8V – 21V LED power)
	30	NC	Reserved (Reserved for EDID test)

(2) CN2 (LED BACKLIGHT)

Input Connector	型式	MS24022P12 (STM) or equivalent 12 pin connector	
Pin assignment	Pin	Signal	Description
	1	VLED	LED power current supply
	2	VLED	LED power current supply
	3	VLED	LED power current supply
	4	NC	No connection
	5	NC	No connection
	6	NC	No connection
	7	NC	No connection
	8	NC	No connection
	9	LED1	LED stream1 current back in.
	10	LED2	LED stream2 current back in.
	11	LED3	LED stream3 current back in.
	12	LED4	LED stream4 current back in.

【Note】

BIST (Build in self-test pattern)

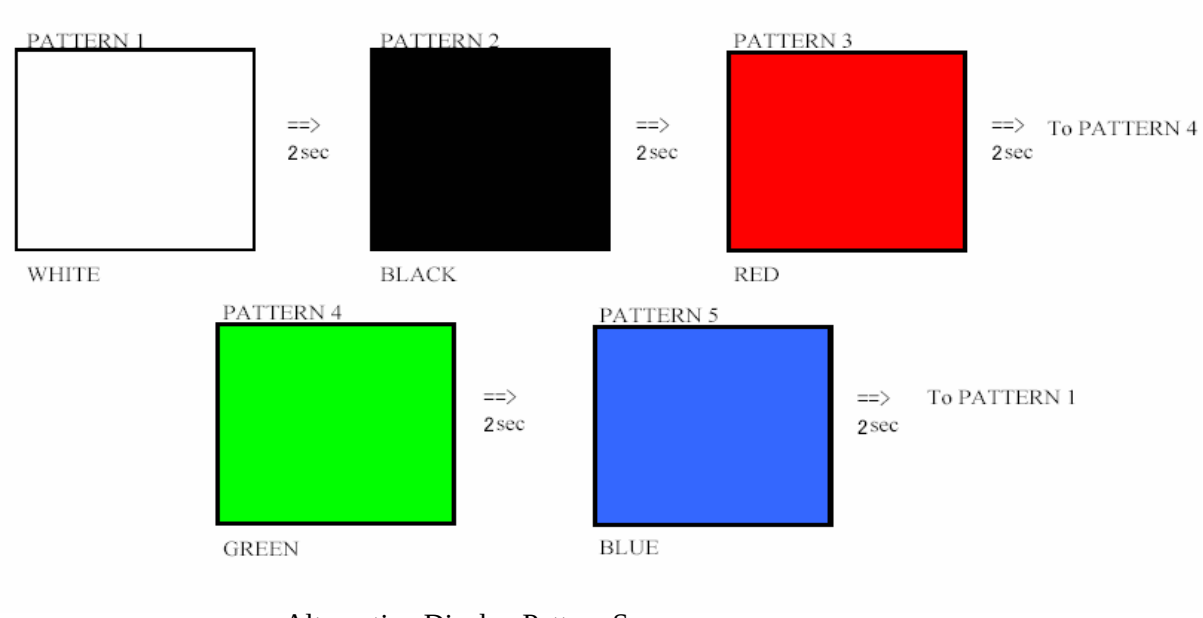
BIST pin = low(GND)：Normal

BIST pin = high(VCC)：Self-test mode

(1). Self-test Display Pattern change when pin 5 is high and no LVDS input signals detected, as followed patterns runs continuously. (White, Black, Red, Green and Blue).

(2). Pattern sequence

Pattern1→ Pattern2→ Pattern3→ Pattern4→ Pattern5→Pattern1→……..

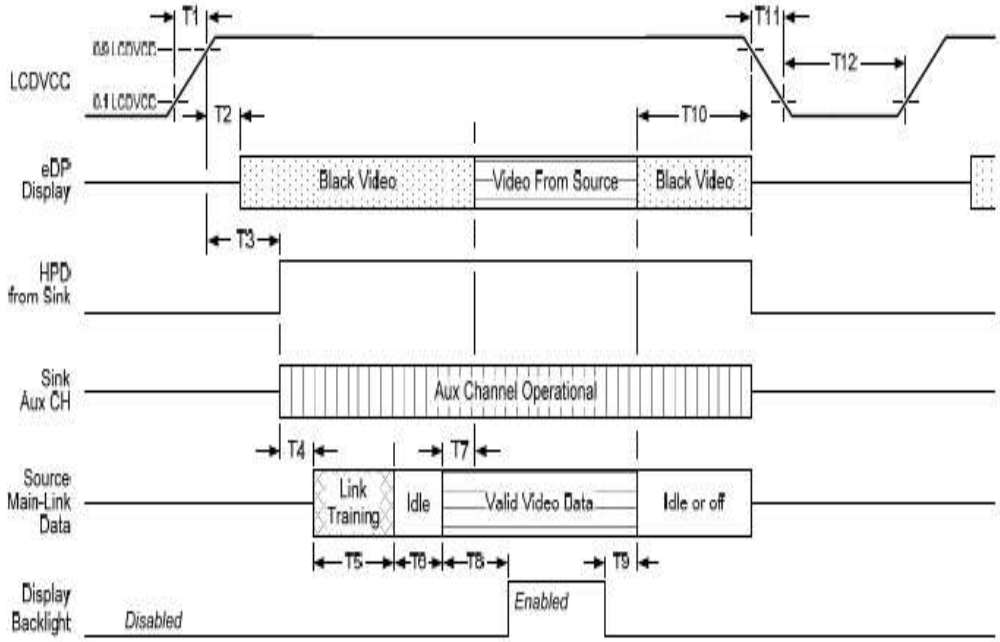


Alternative Display Pattern Sequence

5. INTERFACE TIMING CHART

(1)eDP input time sequence and signal definite：

The VESA Display Port related AC specification is compliant with the specification in the VESA Display Port Standard v1.1a.



Timing Parameter	Description	Reqd. By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	
T2	Delay from LCDVCC to black video generation	Sink	0ms	200ms	Prevents display noise until valid video data is received from the Source (see note 1 below)
T3	Delay from LCDVCC to HPD high	Sink	0ms	200ms	Sink Aux Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max allows Sink validate video data and timing
T8	Delay from valid video data from Source to backlight enable	Source	-	-	Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	Source must assure backlight is no longer illuminated (see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T11	Power rail fall time, 90% to 10%	Source	-	10ms	
T12	Power off time	Source	500ms	-	

(2) Timing Chart

ITEM				SYNBOL	MIN	TYP	MAX	UNIT
LCD Timing	Frame Rate			-	55	60	60	Hz
	DCLK		Frequency	f_{CLK}	88.04	97.78	108	MHz
			Period	t_{CLK}	11.35	10.22	9.26	ns
	DENA	Horizontal	Horizontal total time	t_H	1740	1760	1800	t_{CLK}
			Horizontal Active time	t_{HA}	1600	1600	1600	t_{CLK}
			Horizontal Blank time	t_{HB}	140	160	200	t_{CLK}
		Vertical	Vertical total time	t_V	920	926	1000	t_H
			Vertical Active time	t_{VA}	900	900	900	t_H
			Vertical Blank time	t_{VB}	20	26	100	t_H

【Note】

*1) DENA (DATA ENABLE) usually is positive.

*2) During the whole blank period, DCLK should keep input.

(3) DATA mapping

Color	Input Data	R DATA						G DATA						B DATA					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

【Note】

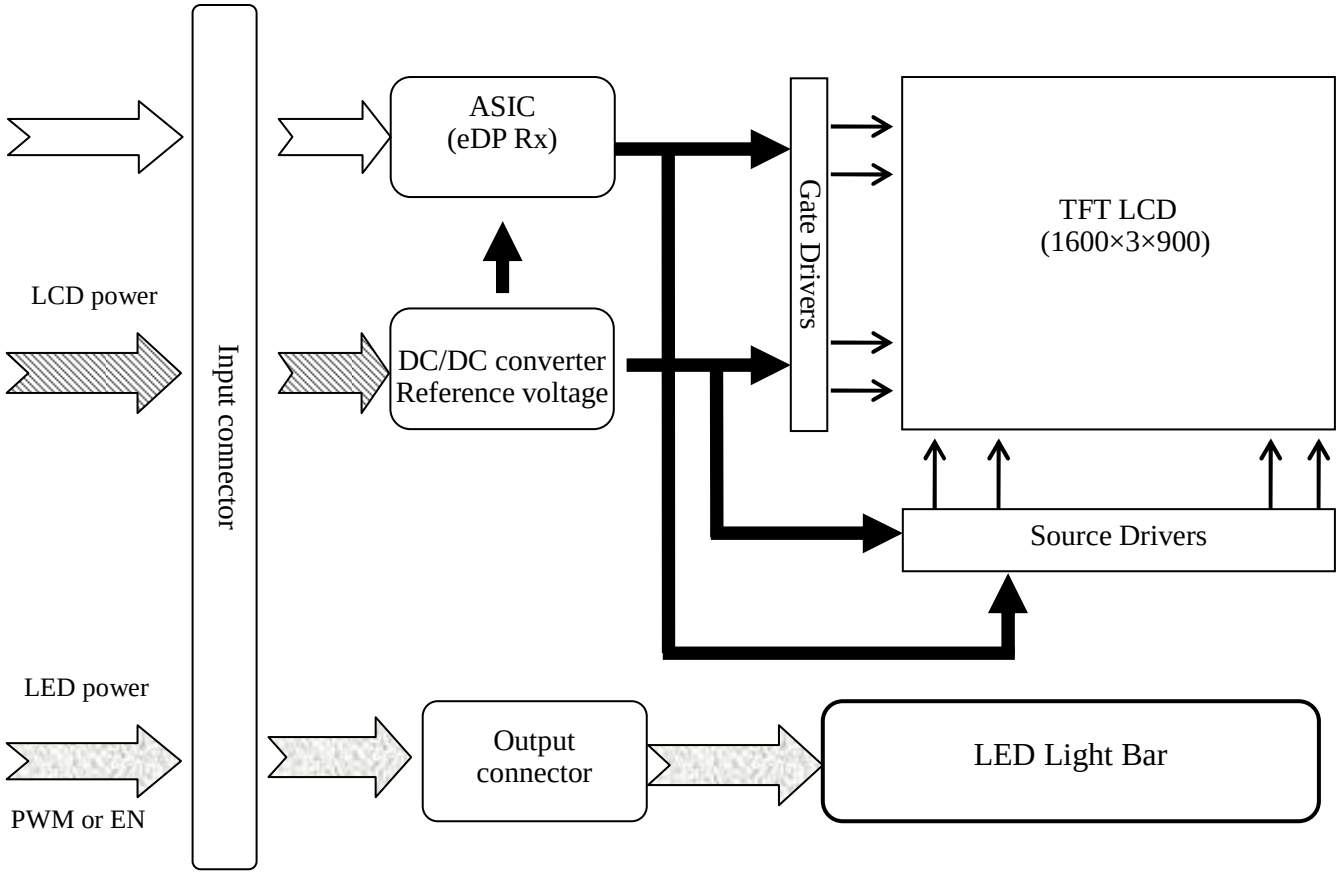
1) Gray level:

Color(n)：n is level order; higher n means brighter level.

2) DATA:

1: high，0: low

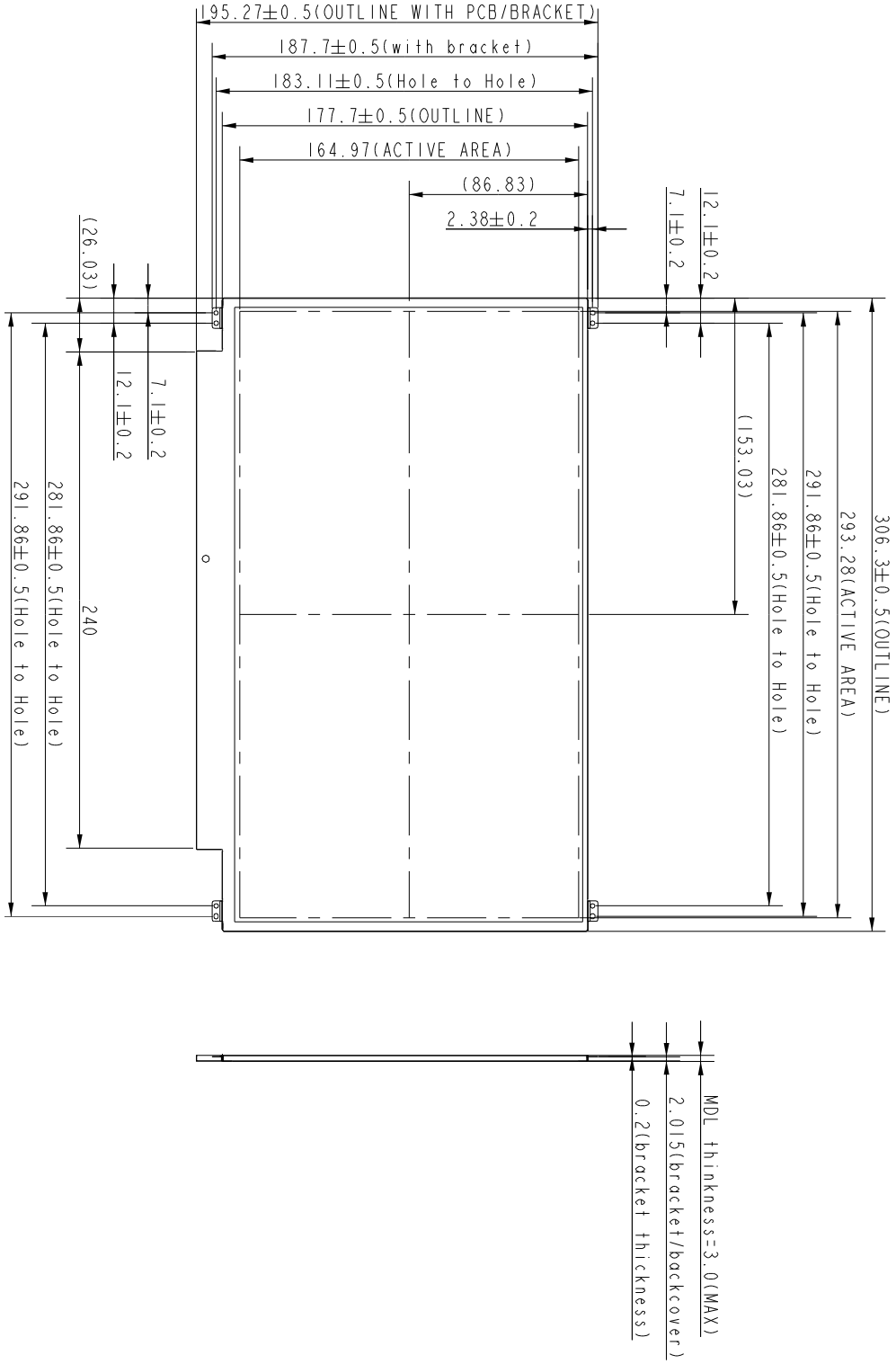
6. BLOCK DIAGRAM



7. MECHANICAL SPECIFICATION

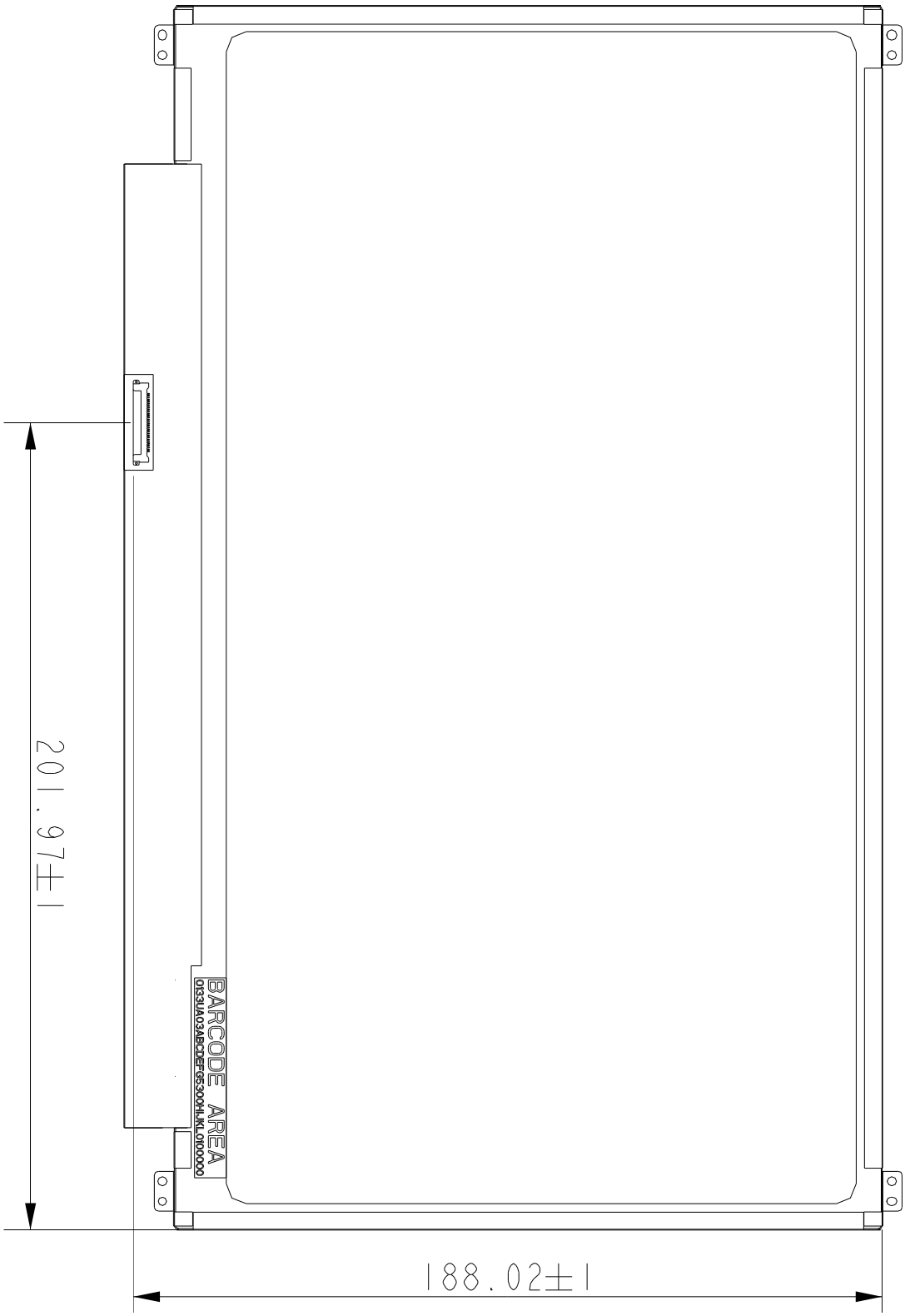
(1) Front side

The tolerance, not show in the figure, is ±0.5 mm. **[Unit：mm]**



(2) Rear side

The tolerance, not show in the figure, is ±0.5 mm. **[Unit：mm]**


201.97±1
188.02±1
BARCODE AREA
0133UA03AB3CDEFG300HMLJ0000000

8. OPTICAL CHARACTERISTICS

Ta=25℃，VDD=3.3V

ITEM		SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
Contrast Ratio		CR	θ＝ψ= 0°	300	400		--	*1) 2)
Luminance (5P)		L	θ＝ψ= 0°	250	290		cd/m^2	*1) 3)
Uniformity(5P)		ΔL	θ＝ψ= 0°	80			%	*1) 3)
Uniformity(13P)		ΔL	θ＝ψ= 0°	65			%	*1) 3)
Response Time		Tr	θ＝ψ= 0°		6	9	ms	*5)
		Tf	θ＝ψ= 0°		10	16	ms	*5)
Cross Talk		CT	θ＝ψ= 0°			1	%	*6)
View Angle	Horizontal	ψ	CR≧10	80/-80			°	*4)
	Vertical	θ		60/-80			°	*4)
Color Temperature Coordinate	W	X	θ＝ψ= 0°	0.293	0.313	0.333		*3)
		Y		0.309	0.329	0.349		
	R	X		TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
	G	X		TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
	B	X		TBD	TBD	TBD		
		Y		TBD	TBD	TBD		
Gamut			θ＝ψ= 0°	42%	45%			
Gamma		γ	GL	2.0	2.2	2.4		*7)

Color coordinate and color gamut are measured by SRUL1R, response time is measured by TRD-100, and all the other items are measured by BM-5A (TOPCON). All these items are measured under the dark room condition (no ambient light).

Measurement Condition: IL= 20mA (each LED)

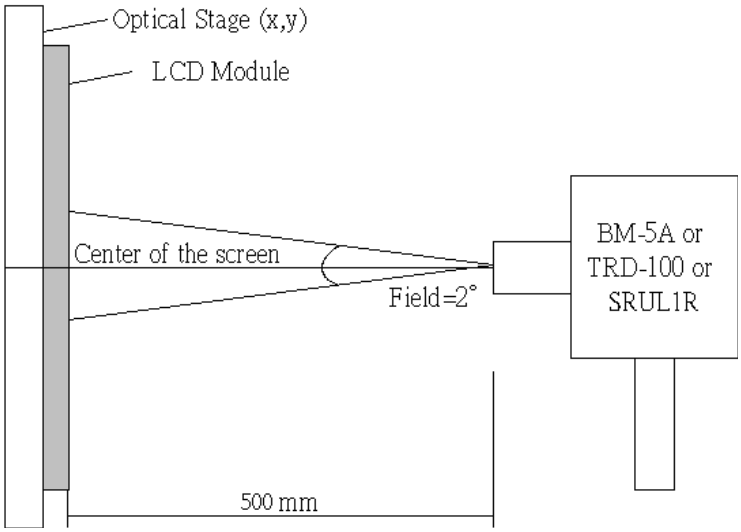
Definition of these measurement items is as follows:

***1) Setup of Measurement Equipment**

The LCD module should be turn-on to a stable luminance level to be reached. The measurement should be executed after lighting Backlight for 20 minutes and in a dark room.

***2) Definition of Contrast Ratio**

CR=ON (White) Luminance/OFF (Black) Luminance



***3) Definition of Luminance and Luminance uniformity**

Central luminance: The white luminance is measured at the center position "5" on the screen, see Fig.1 below.

5P Luminance (AVG): The white luminance is measured at measuring points 5、10、11、12、13, see Fig.1 below.

5P Uniformity: Δ L = (Lmin / Lmax) ×100%

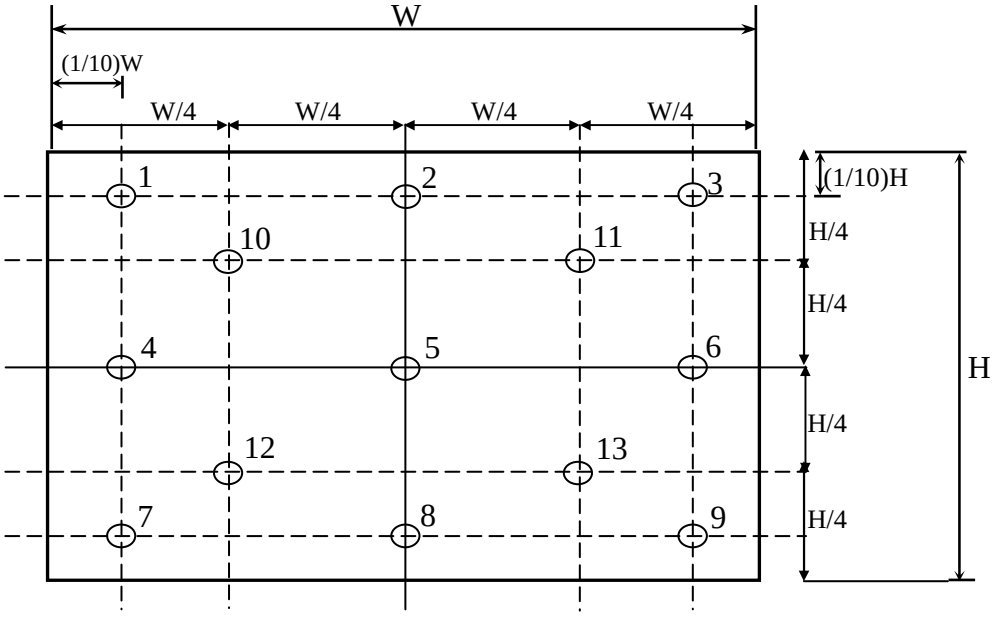
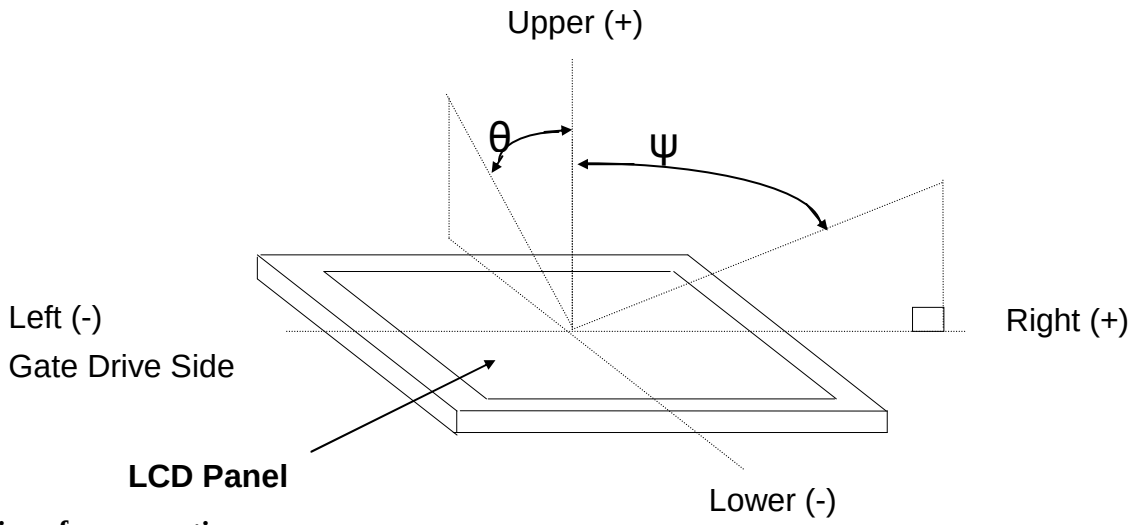
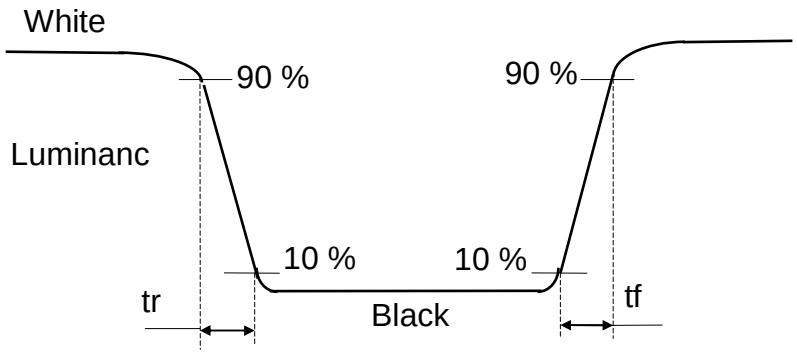


Fig.1 Measure point (Active area)

***4) Definition of view angle(θ，ψ)**



***5) Definition of response time**



***6) Crosstalk Modulation Ratio:**

CT=｜Y_B-Y_A｜ / Y_A×× 100%

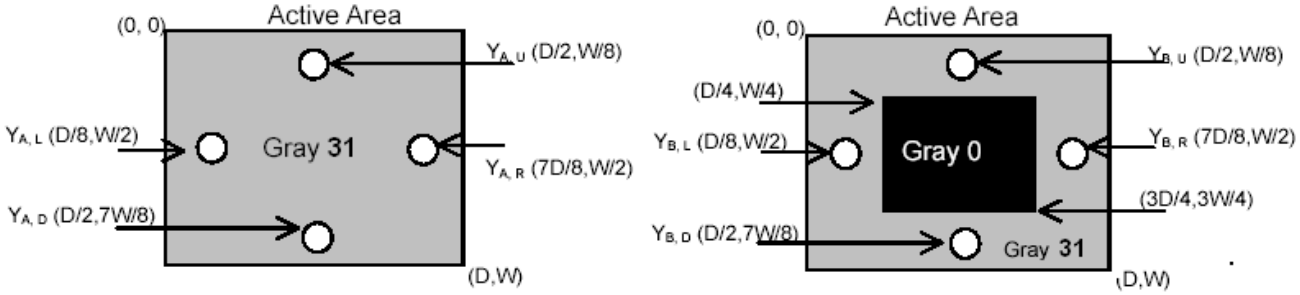
Y_A、Y_B measure position and definition

Y_A means luminance at gray level 31(exclude gray level 0 pattern)

Y_B means luminance at gray level 31(include gray level 0 pattern)

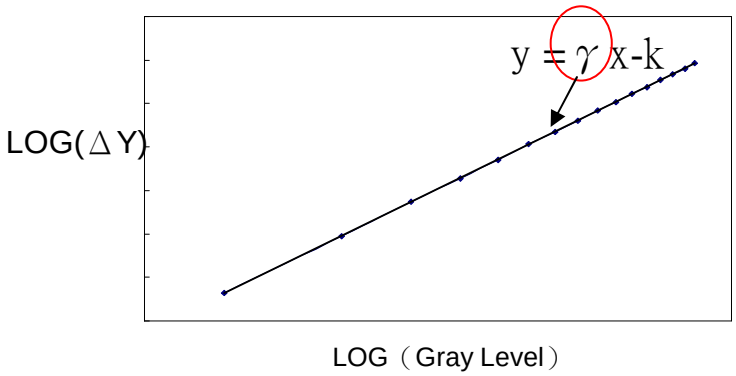
White：63 Gray

Black：0 Gray



***7) Definition of Gamma (VESA)**

Based on Customer Sample, take the average value as a standard center value and the variation range of gamma value caused by loop voltage error should be between +/- 0.2. the bellow figure shows how to obtain the gamma curve and γ (from gray level: 0、4、8-----60、63).



9. RELIABILITY TEST CONDITIONS

(1) Temperature and Humidity

TEST ITEMS	CONDITIONS
High Temperature Operation	50°C ；250Hrs
High Temperature Storage	65°C ；250Hrs
High Temperature High Humidity Operation	40°C ；95% RH；250Hrs
High Temperature High Humidity Storage	60°C ；90% RH；48 Hrs
Low Temperature Operation	0°C ；250 Hrs
Low Temperature Storage	-30°C ；250 Hrs
Thermal Shock	-40°C (0.5 Hr)～65°C (0.5 Hr), Ramp<20°C, 100 CYCLES
Temperature & Pressure Storage	-30°C ；260hPa，24 Hrs

(2) Shock & Vibration

TEST ITEMS	CONDITIONS
Shock (Non-Operation)	210G, 3ms, half sine wave, ± X,± Y,± Z 1time each
Vibration (Non-Operation)	Vibration level : 14.7m/s^2 (1.5G), sinusoidal wave (each x, y, z axis : 1hr, total 3hrs) Frequency range : 5～500 Hz Sweep speed : 0.5 Octave/min.

(3) ESD

	Surface discharge(Panel display area、Frame、PWB、Panel back side)		Electrics capacity of Connector
	Contact	Air	Contact
Capacity	150 pF	150 pF	200 pF
Resistance	330 Ω	330 Ω	0 Ω
Voltage	±8kV	±8kV/±15kV	±250 V
Interval	1 sec	1 sec	1 sec
Times(single point)	25	25	1

(4) MTBF without B/L: 200,000 Hrs (min) lifetimes.

(5) Judgment standard

The judgment of the above test should be made as follow:

Pass：Normal display image with no obvious non-uniformity and no line defect.

Partial transformation of the module parts should be ignored.

Fail：No display image, obvious non-uniformity, or line defects.